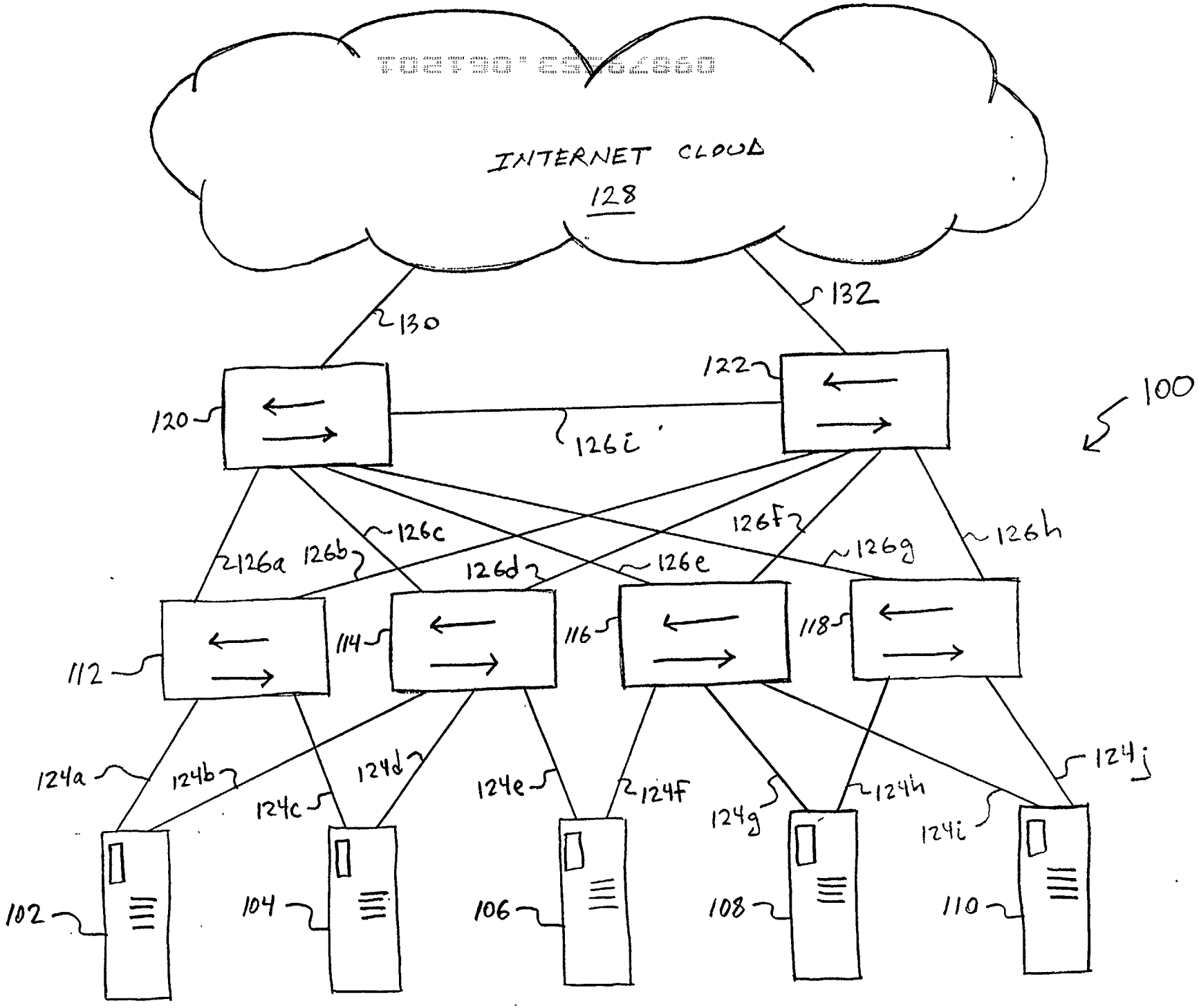
INTERNET CLOUD
128
130
132
120
122
126i
100
126a
126b
126c
126d
126e
126F
126g
126h
112
114
116
118
124a
124b
124c
124d
124e
124F
124g
124h
124i
124j
102
104
106
108
110

FIG. 1

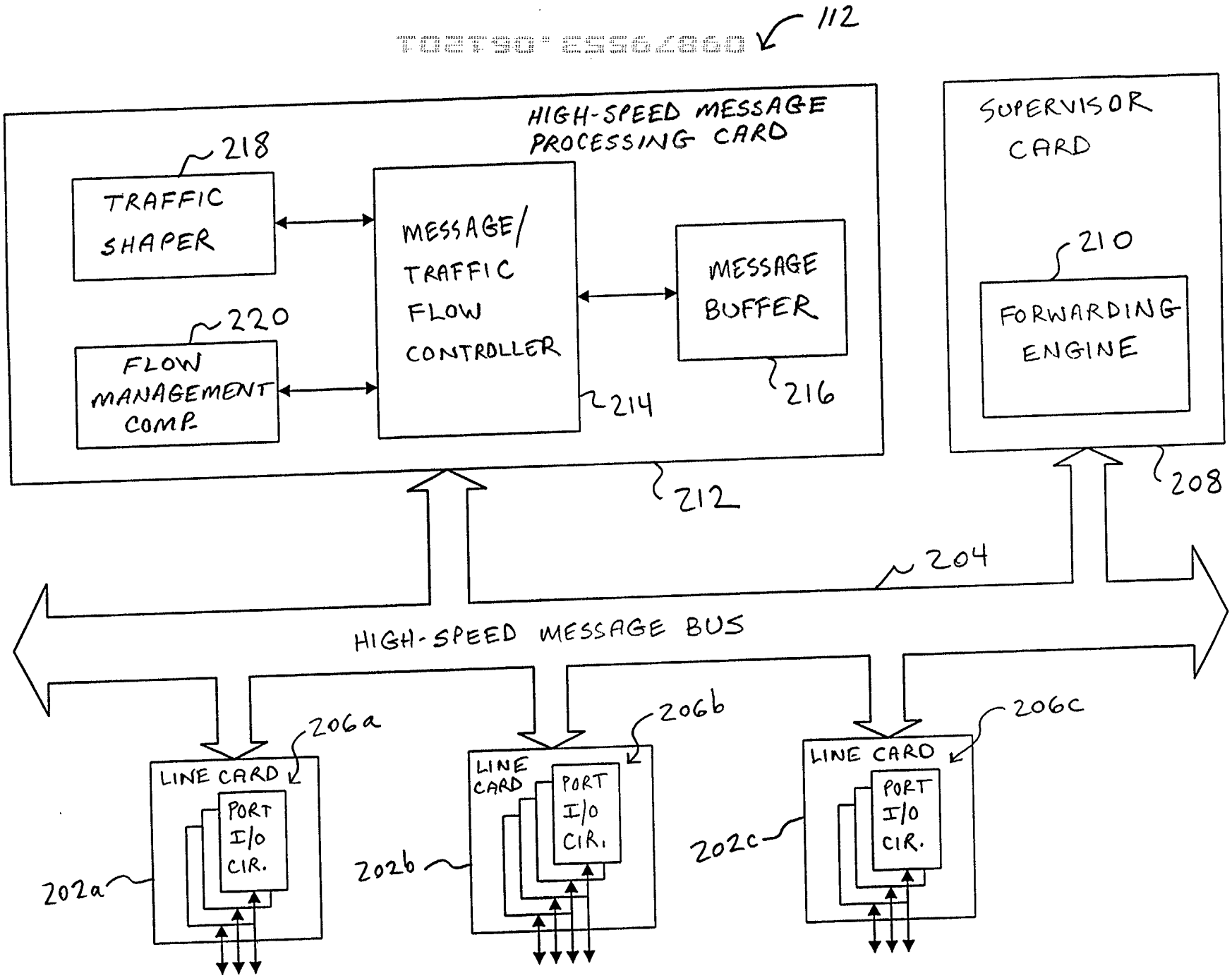
112
HIGH-SPEED MESSAGE PROCESSING CARD
218
TRAFFIC SHAPER
220
FLOW MANAGEMENT COMP.
MESSAGE/ TRAFFIC FLOW CONTROLLER
214
MESSAGE BUFFER
216
212
SUPERVISOR CARD
210
FORWARDING ENGINE
208
204
HIGH-SPEED MESSAGE BUS
206a
LINE CARD
PORT I/O CIR.
202a
206b
LINE CARD
PORT I/O CIR.
202b
206c
LINE CARD
PORT I/O CIR.
202c

FIG. 2

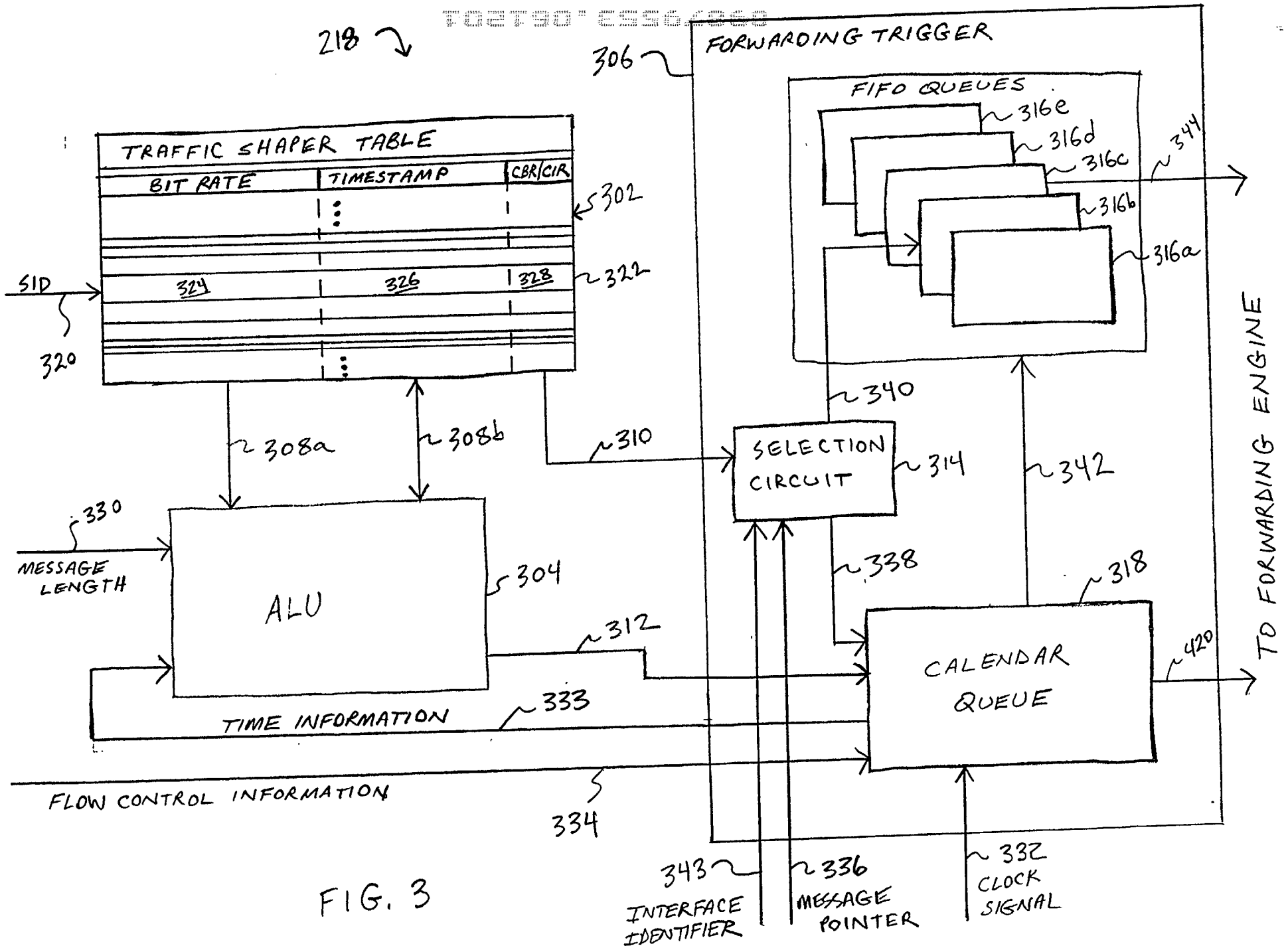
218
306
FORWARDING TRIGGER
FIFO QUEUES
316e
316d
316c
316b
316a
344
TRAFFIC SHAPER TABLE
BIT RATE
TIMESTAMP
CBR/CIR
302
SID
320
324
326
328
322
340
308a
308b
310
SELECTION CIRCUIT
314
342
330
MESSAGE LENGTH
ALU
304
338
318
312
CALENDAR QUEUE
420
TO FORWARDING ENGINE
TIME INFORMATION
333
FLOW CONTROL INFORMATION
334
343
INTERFACE IDENTIFIER
336
MESSAGE POINTER
332
CLOCK SIGNAL

FIG. 3

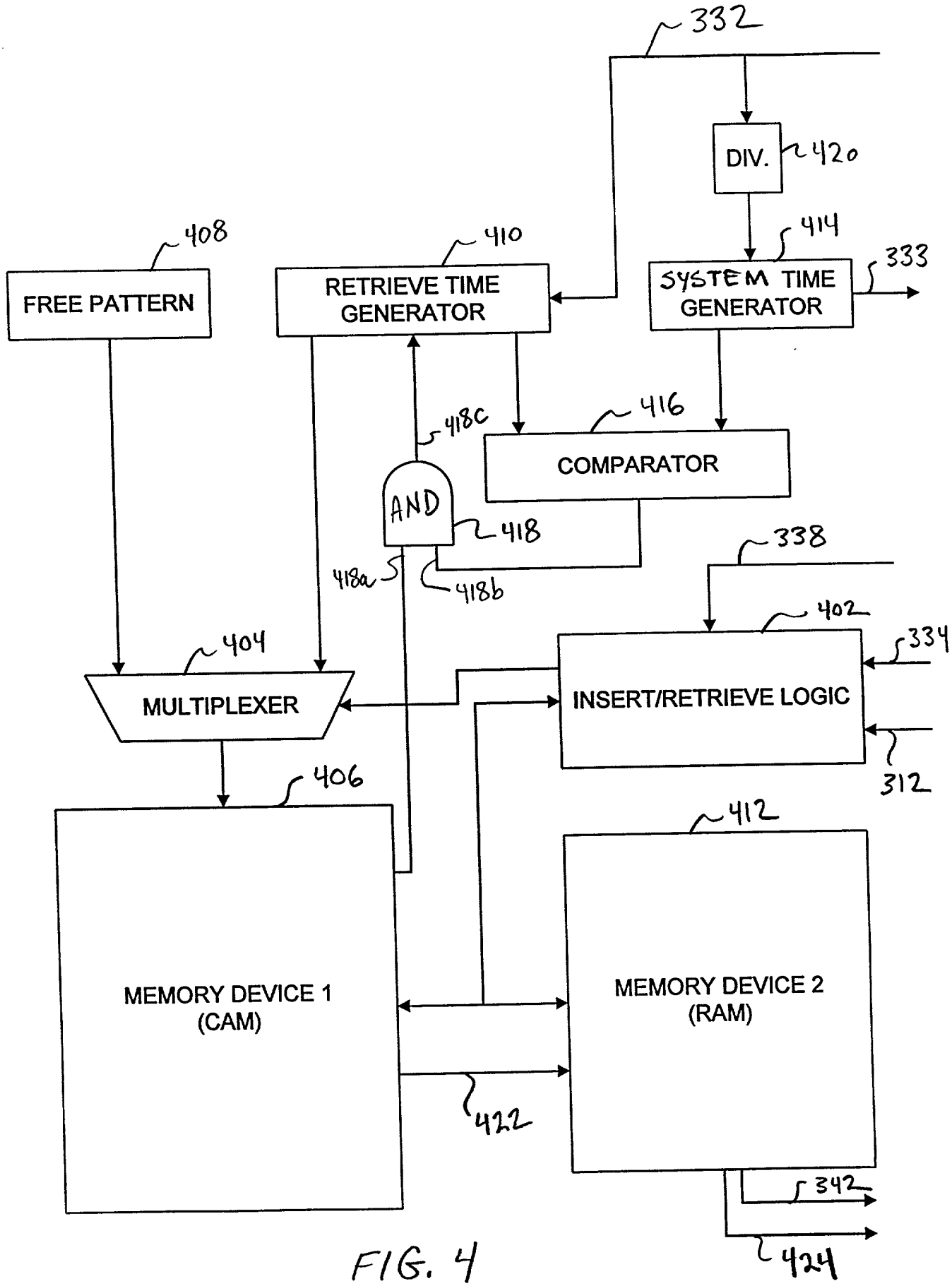
332
DIV.
420
414
333
408
410
FREE PATTERN
RETRIEVE TIME GENERATOR
SYSTEM TIME GENERATOR
418c
416
COMPARATOR
AND
418
338
418a
418b
402
334
404
MULTIPLEXER
INSERT/RETRIEVE LOGIC
312
406
412
MEMORY DEVICE 1 (CAM)
MEMORY DEVICE 2 (RAM)
422
342
424

FIG. 4

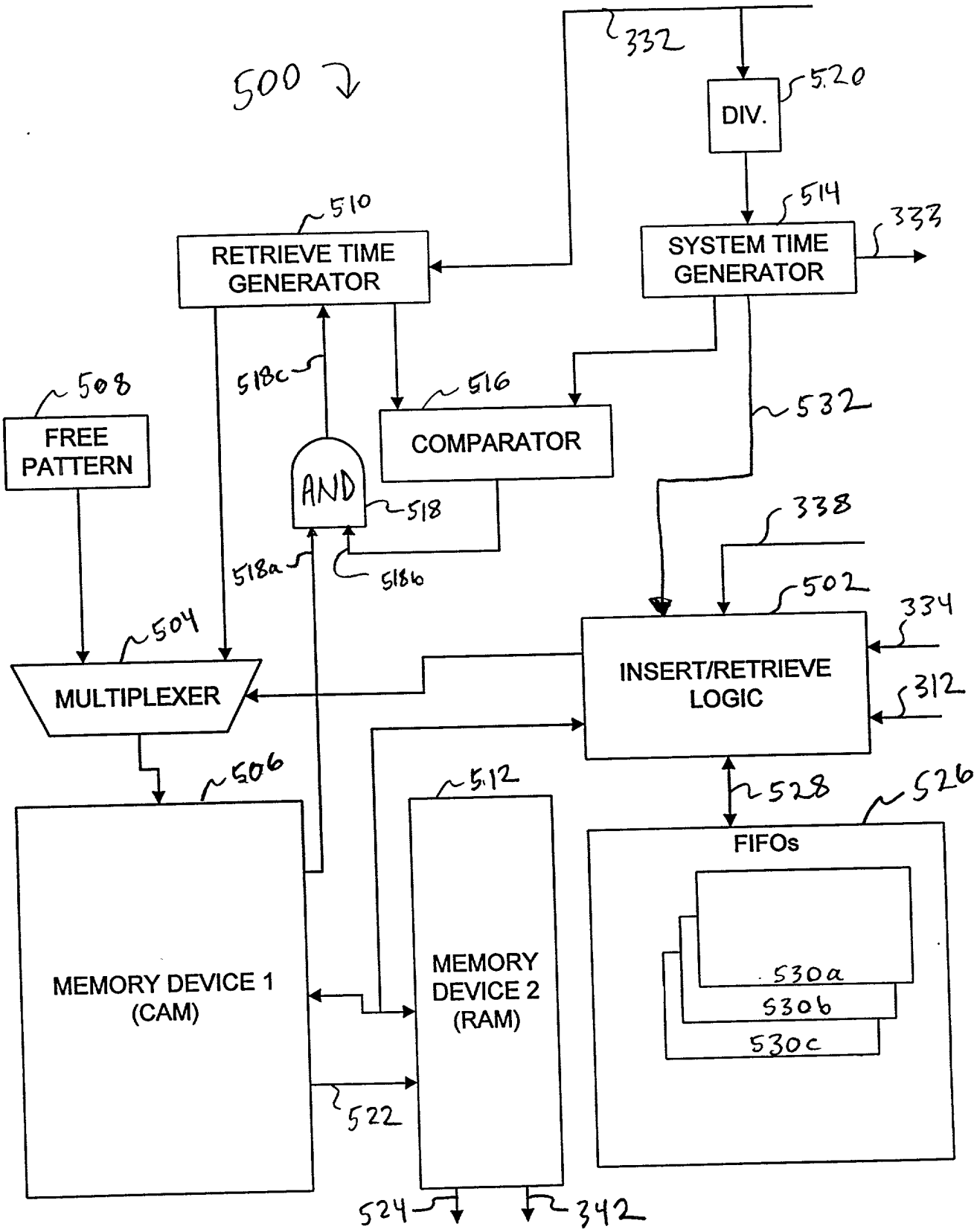
500
332
DIV.
520
514
333
RETRIEVE TIME GENERATOR
510
SYSTEM TIME GENERATOR
508
FREE PATTERN
518c
516
COMPARATOR
532
AND
518
338
518a
518b
502
334
INSERT/RETRIEVE LOGIC
504
MULTIPLEXER
312
506
512
528
526
FIFOs
MEMORY DEVICE 1 (CAM)
MEMORY DEVICE 2 (RAM)
530a
530b
530c
522
524
342

FIG. 5

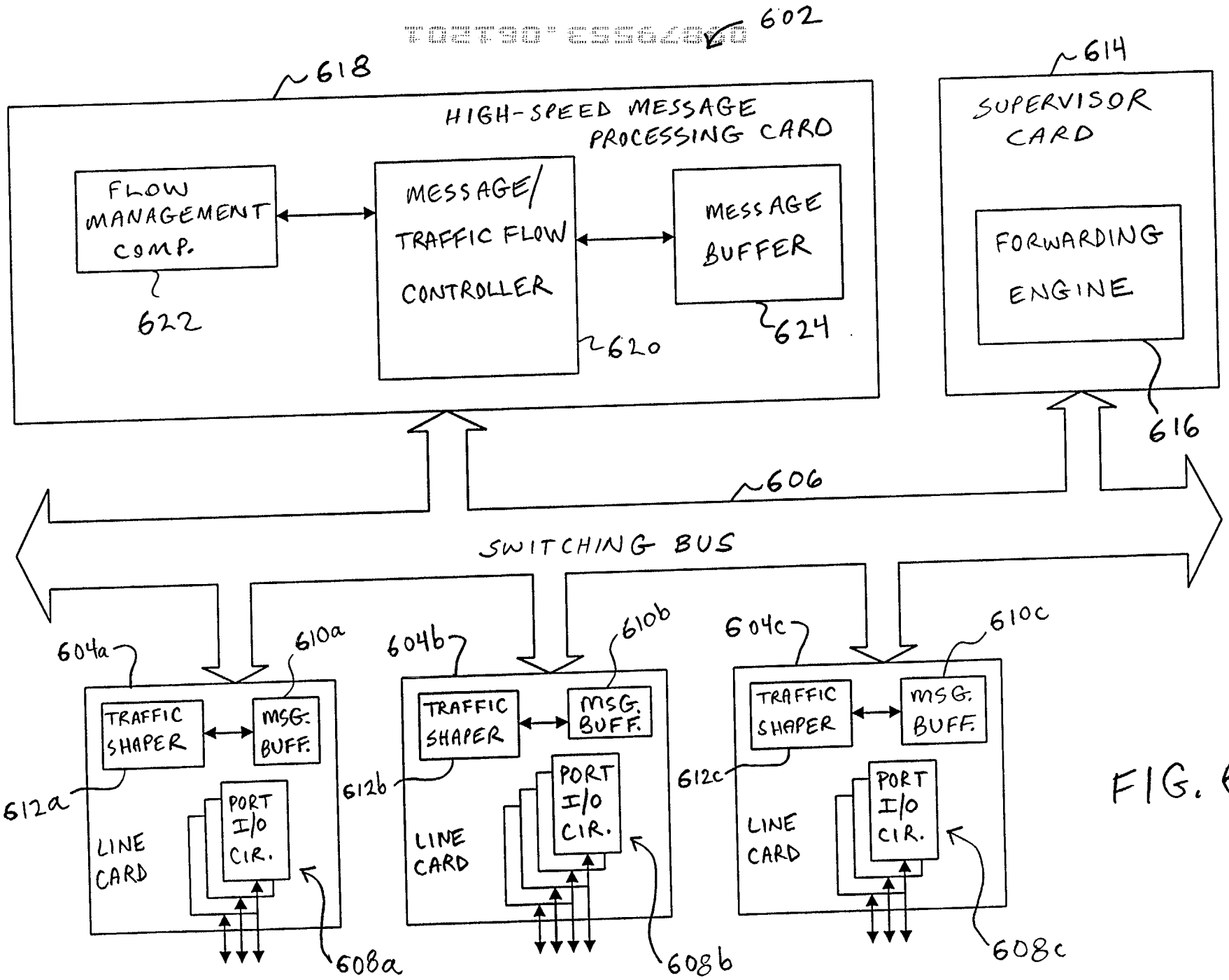
602
618
HIGH-SPEED MESSAGE PROCESSING CARD
FLOW MANAGEMENT COMP.
622
MESSAGE/ TRAFFIC FLOW CONTROLLER
620
MESSAGE BUFFER
624
614
SUPERVISOR CARD
FORWARDING ENGINE
616
606
SWITCHING BUS
604a
610a
TRAFFIC SHAPER
MSG. BUFF.
612a
PORT I/O CIR.
LINE CARD
608a
604b
610b
TRAFFIC SHAPER
MSG. BUFF.
612b
PORT I/O CIR.
LINE CARD
608b
604c
610c
TRAFFIC SHAPER
MSG. BUFF.
612c
PORT I/O CIR.
LINE CARD
608c

FIG. 6

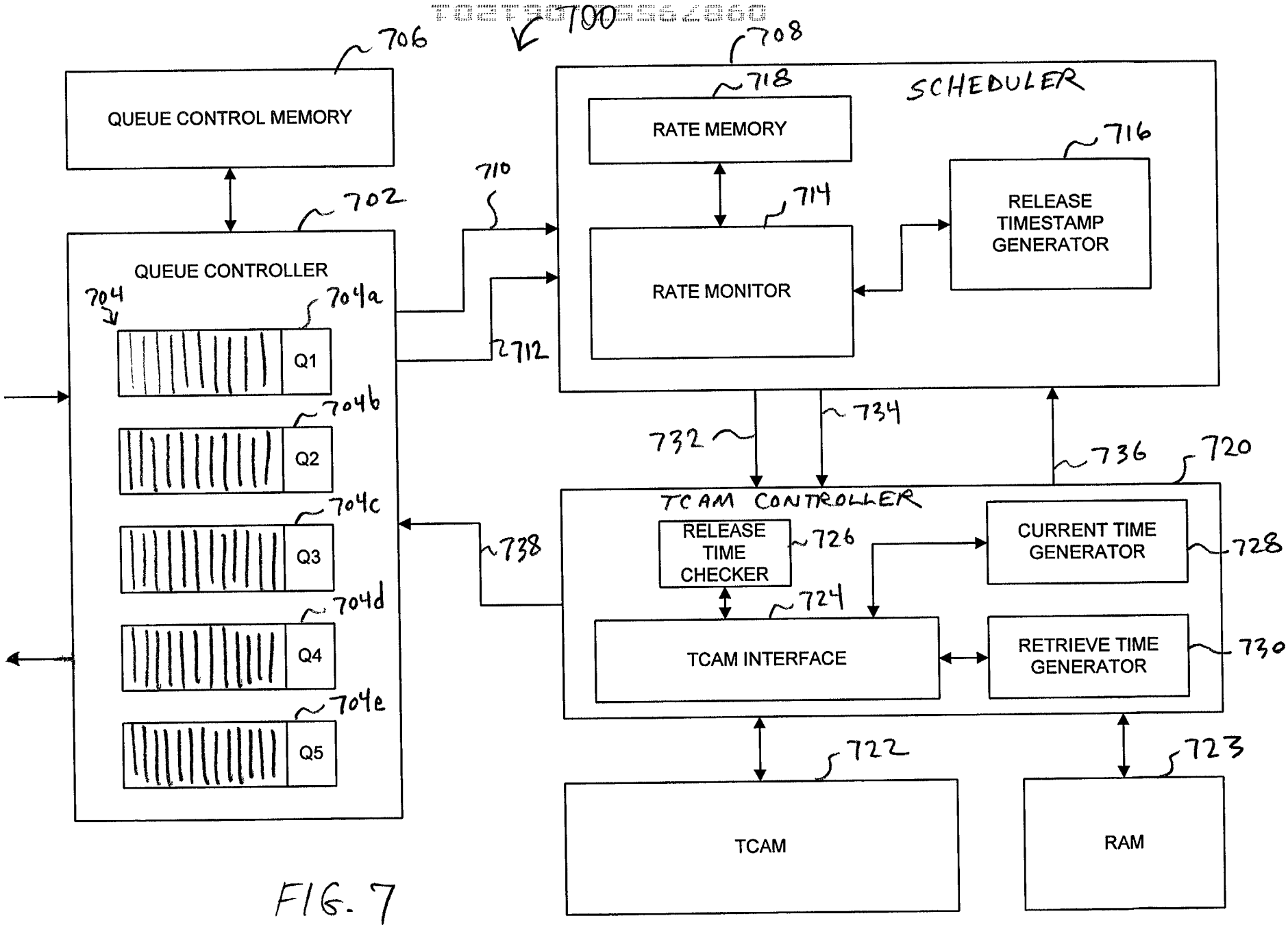
700
706
QUEUE CONTROL MEMORY
708
SCHEDULER
718
RATE MEMORY
716
RELEASE TIMESTAMP GENERATOR
710
714
RATE MONITOR
702
QUEUE CONTROLLER
704
704a
Q1
712
704b
Q2
704c
Q3
704d
Q4
704e
Q5
738
732
734
736
720
TCAM CONTROLLER
RELEASE TIME CHECKER
726
CURRENT TIME GENERATOR
728
724
TCAM INTERFACE
RETRIEVE TIME GENERATOR
730
722
723
TCAM
RAM

FIG. 7

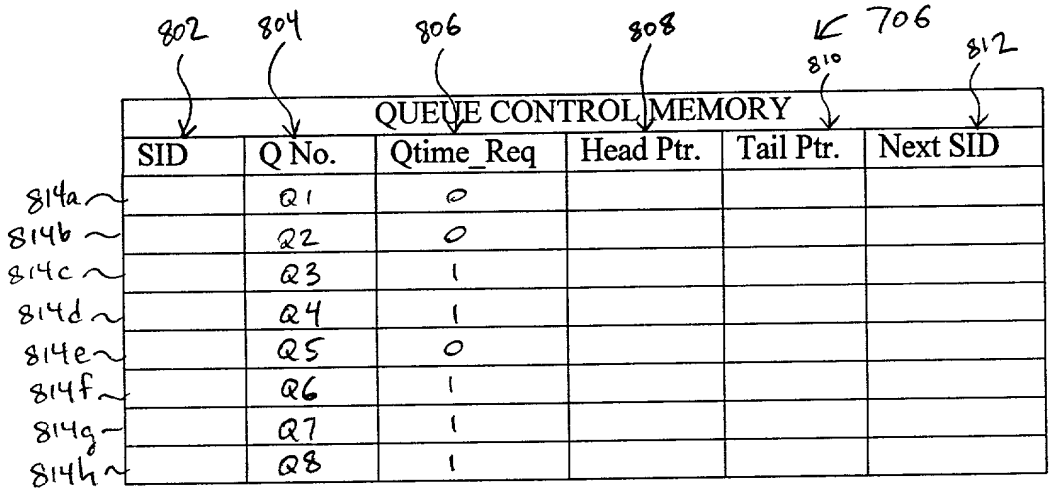
802
804
806
808
706
810
812
QUEUE CONTROL MEMORY
SID
Q No.
Qtime_Req
Head Ptr.
Tail Ptr.
Next SID
814a
814b
814c
814d
814e
814f
814g
814h
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
0
0
1
1
0
1
1
1

FIG. 8

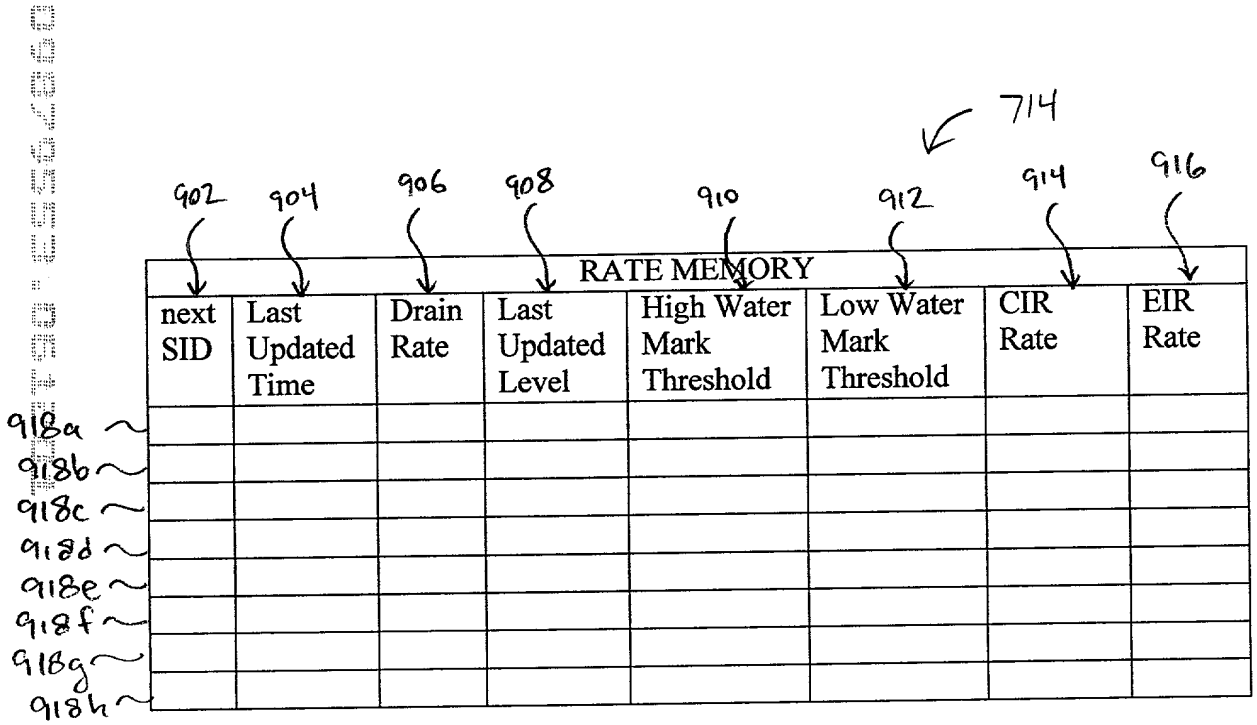
714
902
904
906
908
910
912
914
916
RATE MEMORY
next SID
Last Updated Time
Drain Rate
Last Updated Level
High Water Mark Threshold
Low Water Mark Threshold
CIR Rate
EIR Rate
918a
918b
918c
918d
918e
918f
918g
918h

FIG. 9

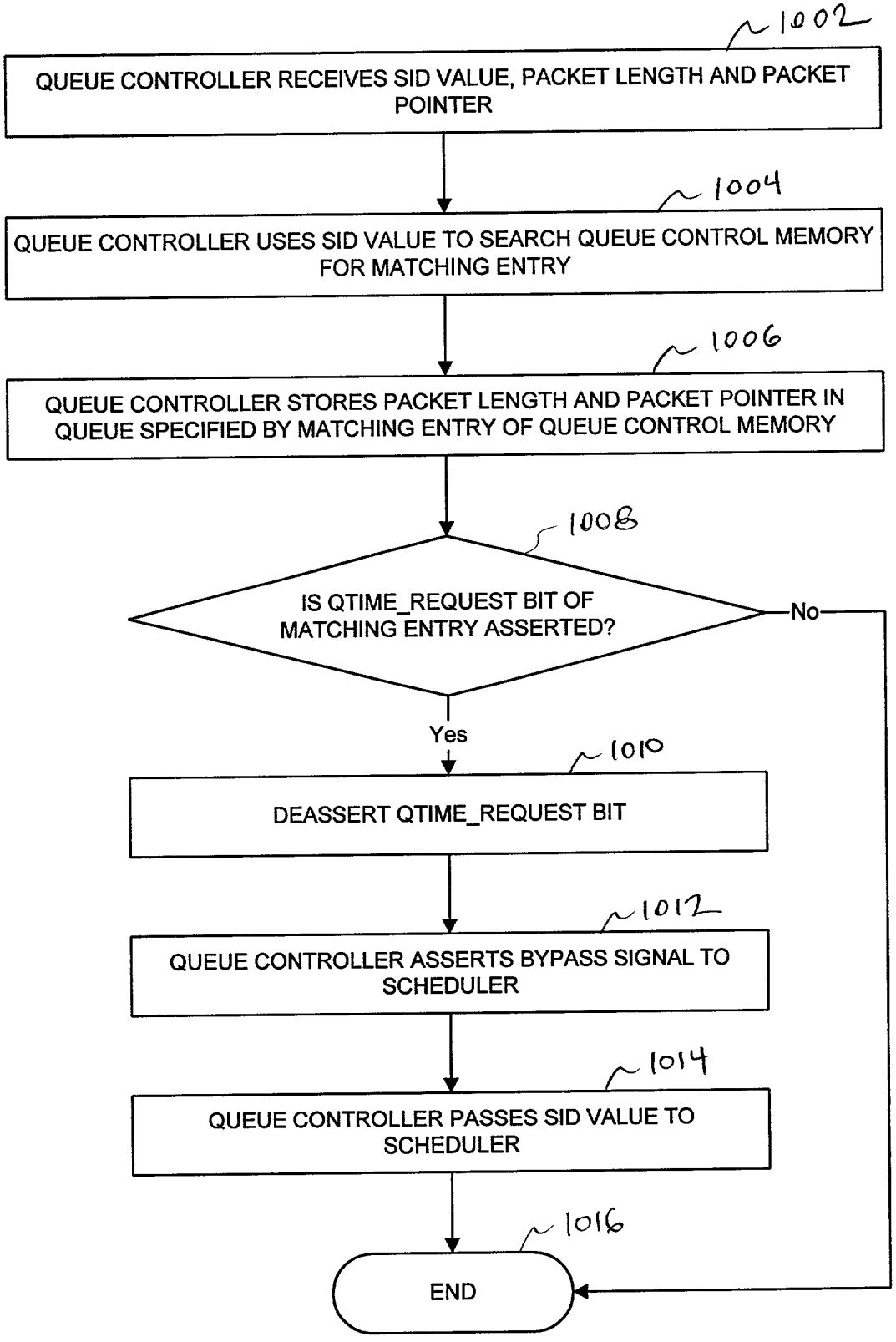
1002
QUEUE CONTROLLER RECEIVES SID VALUE, PACKET LENGTH AND PACKET POINTER
1004
QUEUE CONTROLLER USES SID VALUE TO SEARCH QUEUE CONTROL MEMORY FOR MATCHING ENTRY
1006
QUEUE CONTROLLER STORES PACKET LENGTH AND PACKET POINTER IN QUEUE SPECIFIED BY MATCHING ENTRY OF QUEUE CONTROL MEMORY
1008
IS QTIME_REQUEST BIT OF MATCHING ENTRY ASSERTED?
No
Yes
1010
DEASSERT QTIME_REQUEST BIT
1012
QUEUE CONTROLLER ASSERTS BYPASS SIGNAL TO SCHEDULER
1014
QUEUE CONTROLLER PASSES SID VALUE TO SCHEDULER
1016
END

FIG. 10A

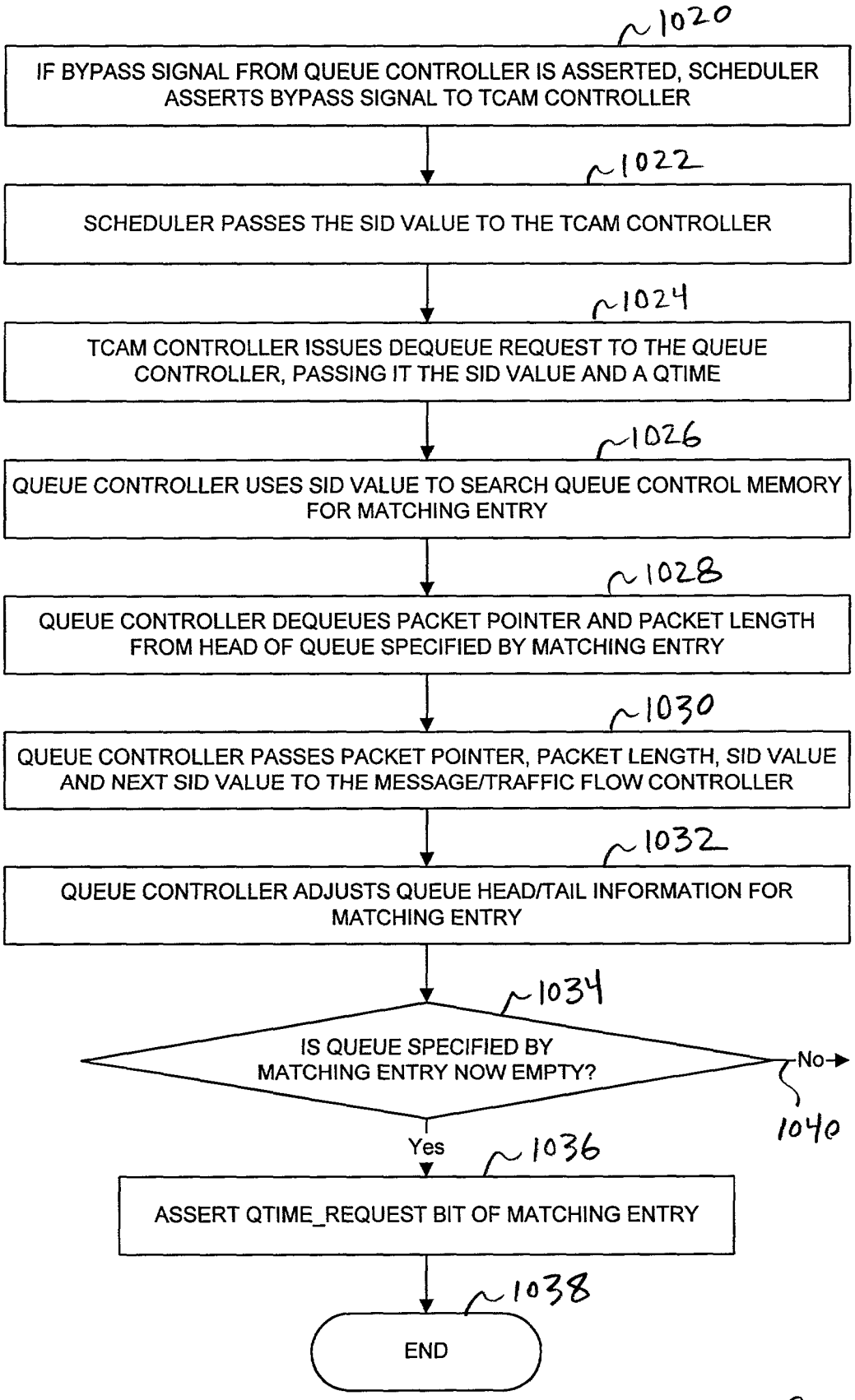
1020
IF BYPASS SIGNAL FROM QUEUE CONTROLLER IS ASSERTED, SCHEDULER ASSERTS BYPASS SIGNAL TO TCAM CONTROLLER
1022
SCHEDULER PASSES THE SID VALUE TO THE TCAM CONTROLLER
1024
TCAM CONTROLLER ISSUES DEQUEUE REQUEST TO THE QUEUE CONTROLLER, PASSING IT THE SID VALUE AND A QTIME
1026
QUEUE CONTROLLER USES SID VALUE TO SEARCH QUEUE CONTROL MEMORY FOR MATCHING ENTRY
1028
QUEUE CONTROLLER DEQUEUES PACKET POINTER AND PACKET LENGTH FROM HEAD OF QUEUE SPECIFIED BY MATCHING ENTRY
1030
QUEUE CONTROLLER PASSES PACKET POINTER, PACKET LENGTH, SID VALUE AND NEXT SID VALUE TO THE MESSAGE/TRAFFIC FLOW CONTROLLER
1032
QUEUE CONTROLLER ADJUSTS QUEUE HEAD/TAIL INFORMATION FOR MATCHING ENTRY
1034
IS QUEUE SPECIFIED BY MATCHING ENTRY NOW EMPTY?
No
1040
Yes
1036
ASSERT QTIME_REQUEST BIT OF MATCHING ENTRY
1038
END

FIG. 10B

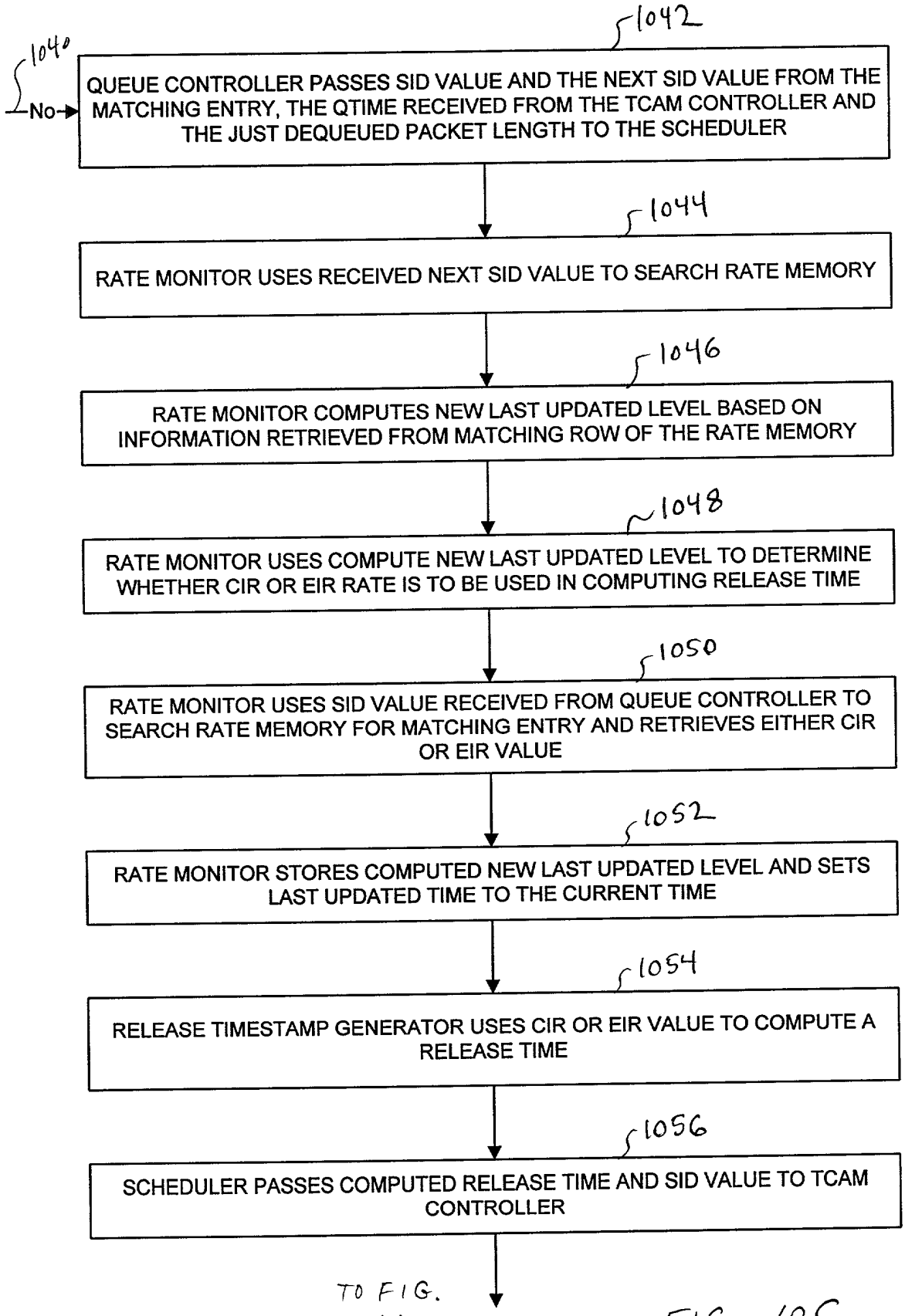
1040
No
1042
QUEUE CONTROLLER PASSES SID VALUE AND THE NEXT SID VALUE FROM THE MATCHING ENTRY, THE QTIME RECEIVED FROM THE TCAM CONTROLLER AND THE JUST DEQUEUED PACKET LENGTH TO THE SCHEDULER
1044
RATE MONITOR USES RECEIVED NEXT SID VALUE TO SEARCH RATE MEMORY
1046
RATE MONITOR COMPUTES NEW LAST UPDATED LEVEL BASED ON INFORMATION RETRIEVED FROM MATCHING ROW OF THE RATE MEMORY
1048
RATE MONITOR USES COMPUTE NEW LAST UPDATED LEVEL TO DETERMINE WHETHER CIR OR EIR RATE IS TO BE USED IN COMPUTING RELEASE TIME
1050
RATE MONITOR USES SID VALUE RECEIVED FROM QUEUE CONTROLLER TO SEARCH RATE MEMORY FOR MATCHING ENTRY AND RETRIEVES EITHER CIR OR EIR VALUE
1052
RATE MONITOR STORES COMPUTED NEW LAST UPDATED LEVEL AND SETS LAST UPDATED TIME TO THE CURRENT TIME
1054
RELEASE TIMESTAMP GENERATOR USES CIR OR EIR VALUE TO COMPUTE A RELEASE TIME
1056
SCHEDULER PASSES COMPUTED RELEASE TIME AND SID VALUE TO TCAM CONTROLLER
TO FIG. 10D

FIG. 10C

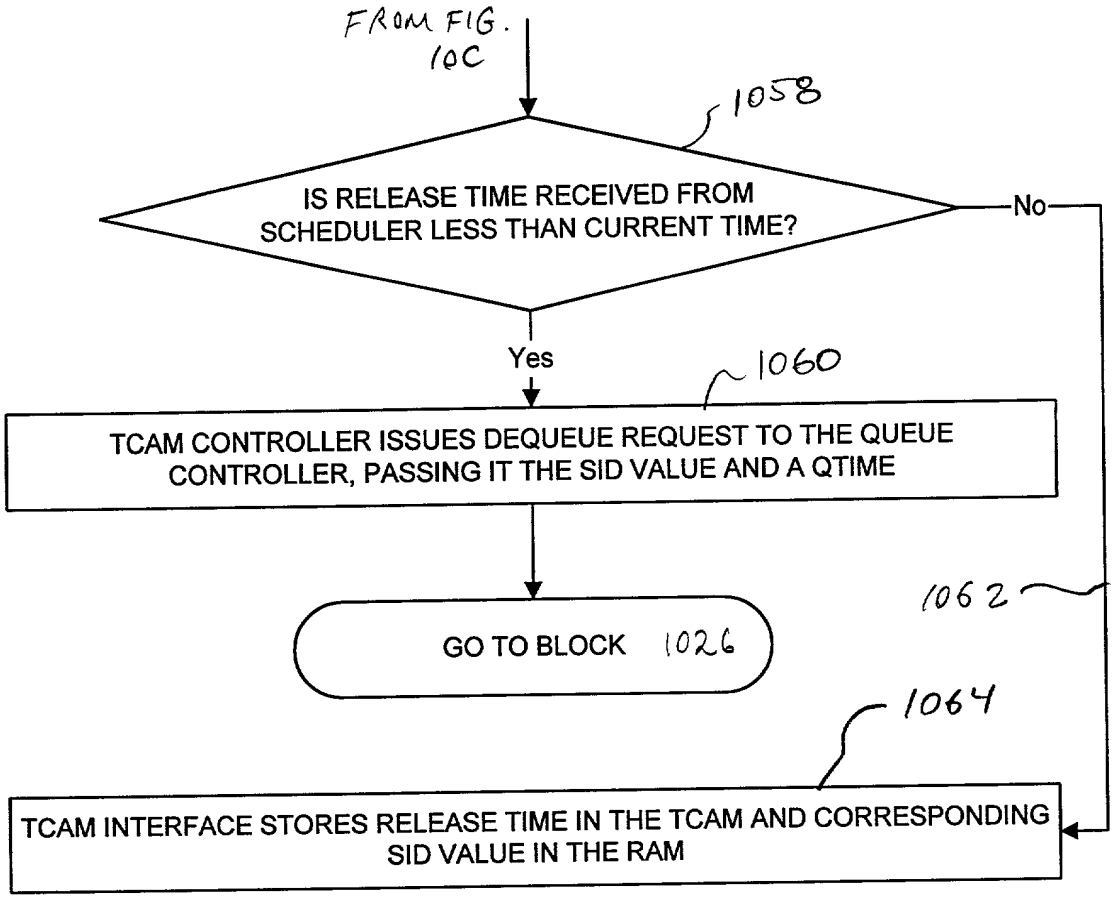
FROM FIG. 10C
1058
IS RELEASE TIME RECEIVED FROM SCHEDULER LESS THAN CURRENT TIME?
No
Yes
1060
TCAM CONTROLLER ISSUES DEQUEUE REQUEST TO THE QUEUE CONTROLLER, PASSING IT THE SID VALUE AND A QTIME
1062
GO TO BLOCK 1026
1064
TCAM INTERFACE STORES RELEASE TIME IN THE TCAM AND CORRESPONDING SID VALUE IN THE RAM

FIG. 10D

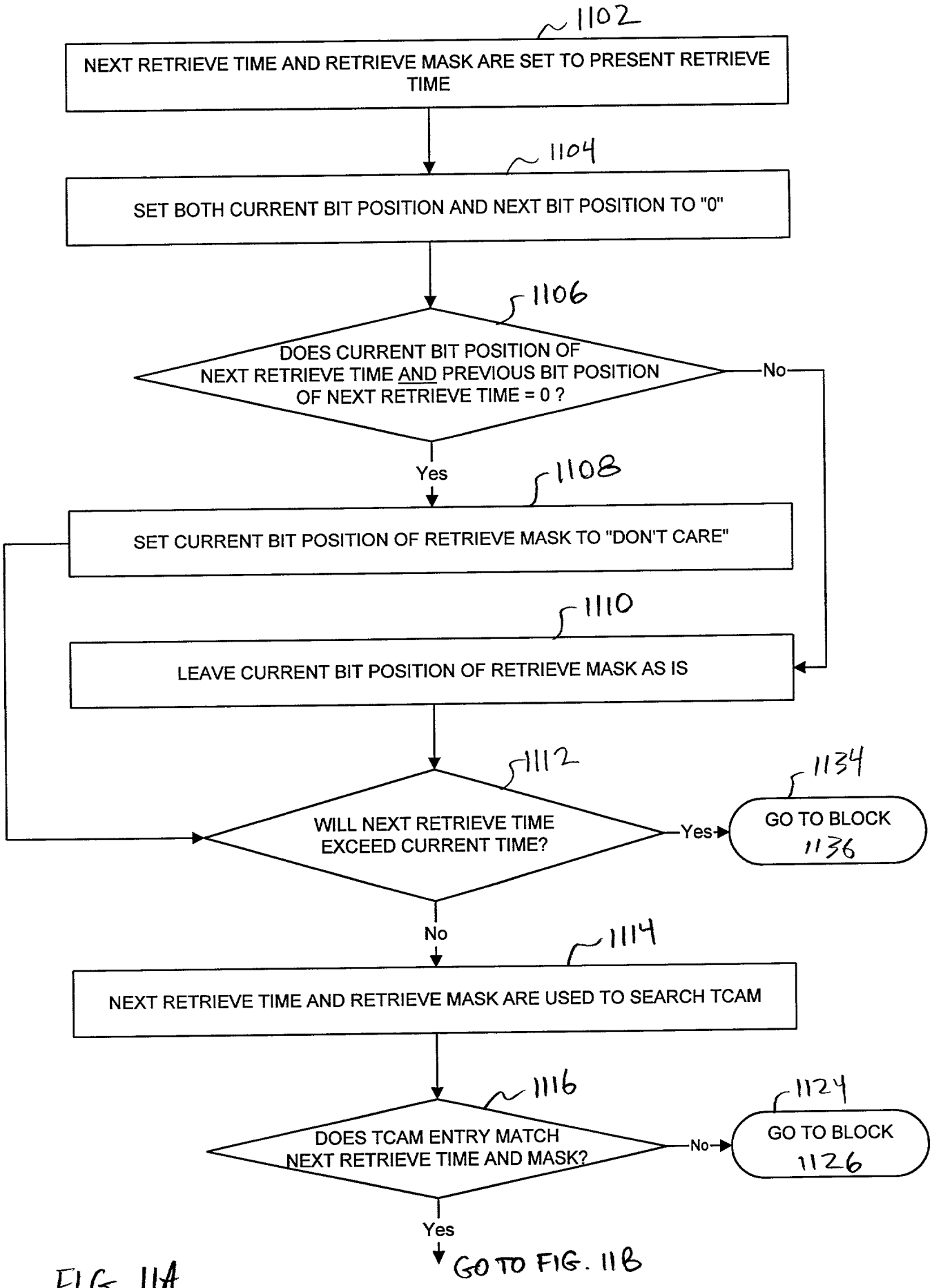
1102
NEXT RETRIEVE TIME AND RETRIEVE MASK ARE SET TO PRESENT RETRIEVE TIME
1104
SET BOTH CURRENT BIT POSITION AND NEXT BIT POSITION TO "0"
1106
DOES CURRENT BIT POSITION OF NEXT RETRIEVE TIME AND PREVIOUS BIT POSITION OF NEXT RETRIEVE TIME = 0 ?
No
Yes
1108
SET CURRENT BIT POSITION OF RETRIEVE MASK TO "DON'T CARE"
1110
LEAVE CURRENT BIT POSITION OF RETRIEVE MASK AS IS
1112
WILL NEXT RETRIEVE TIME EXCEED CURRENT TIME?
Yes
1134
GO TO BLOCK 1136
No
1114
NEXT RETRIEVE TIME AND RETRIEVE MASK ARE USED TO SEARCH TCAM
1116
DOES TCAM ENTRY MATCH NEXT RETRIEVE TIME AND MASK?
No
1124
GO TO BLOCK 1126
Yes
GO TO FIG. 11B

FIG. 11A

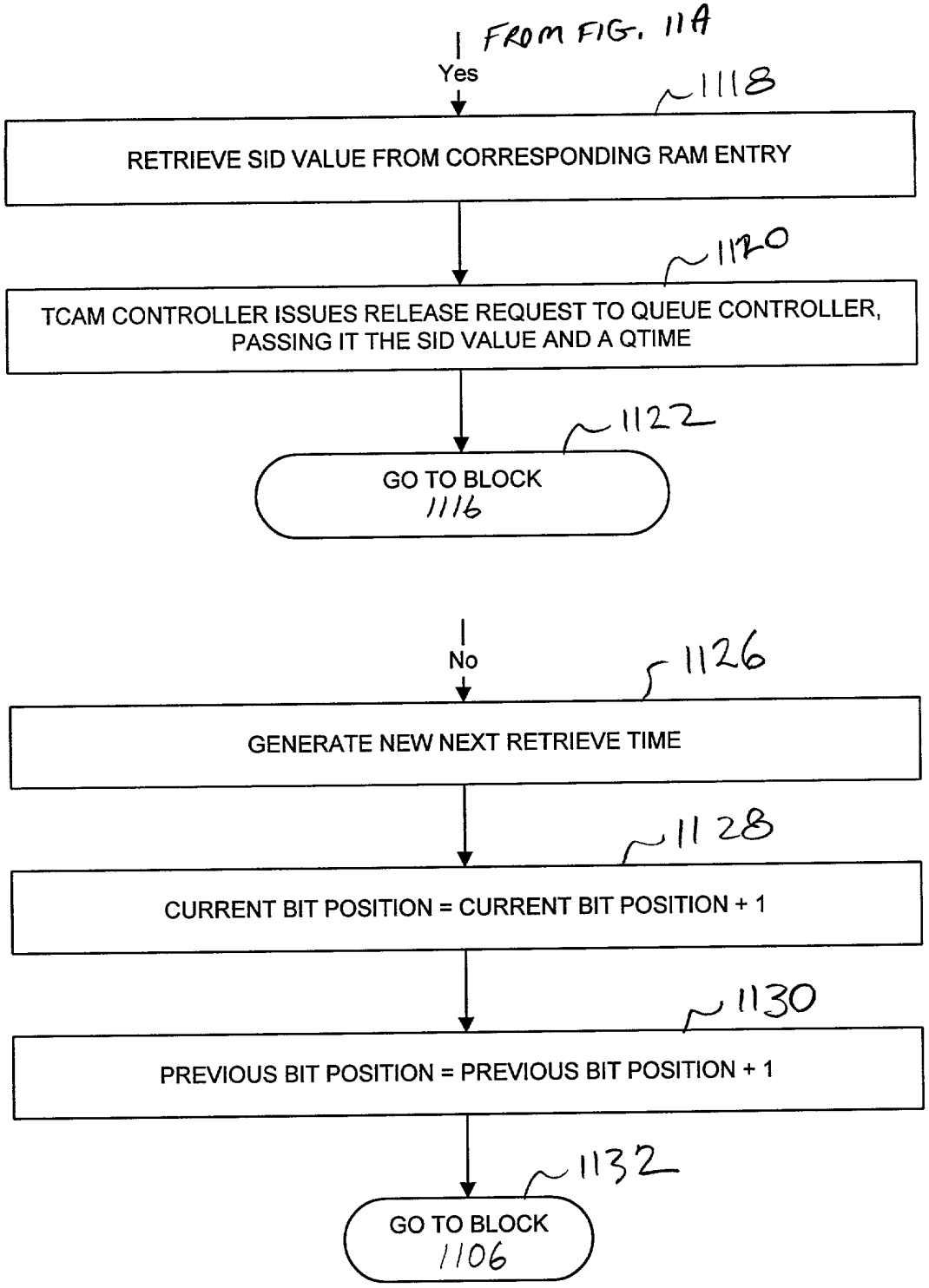
FROM FIG. 11A
Yes
1118
RETRIEVE SID VALUE FROM CORRESPONDING RAM ENTRY
1120
TCAM CONTROLLER ISSUES RELEASE REQUEST TO QUEUE CONTROLLER, PASSING IT THE SID VALUE AND A QTIME
1122
GO TO BLOCK 1116
No
1126
GENERATE NEW NEXT RETRIEVE TIME
1128
CURRENT BIT POSITION = CURRENT BIT POSITION + 1
1130
PREVIOUS BIT POSITION = PREVIOUS BIT POSITION + 1
1132
GO TO BLOCK 1106

FIG. 11B

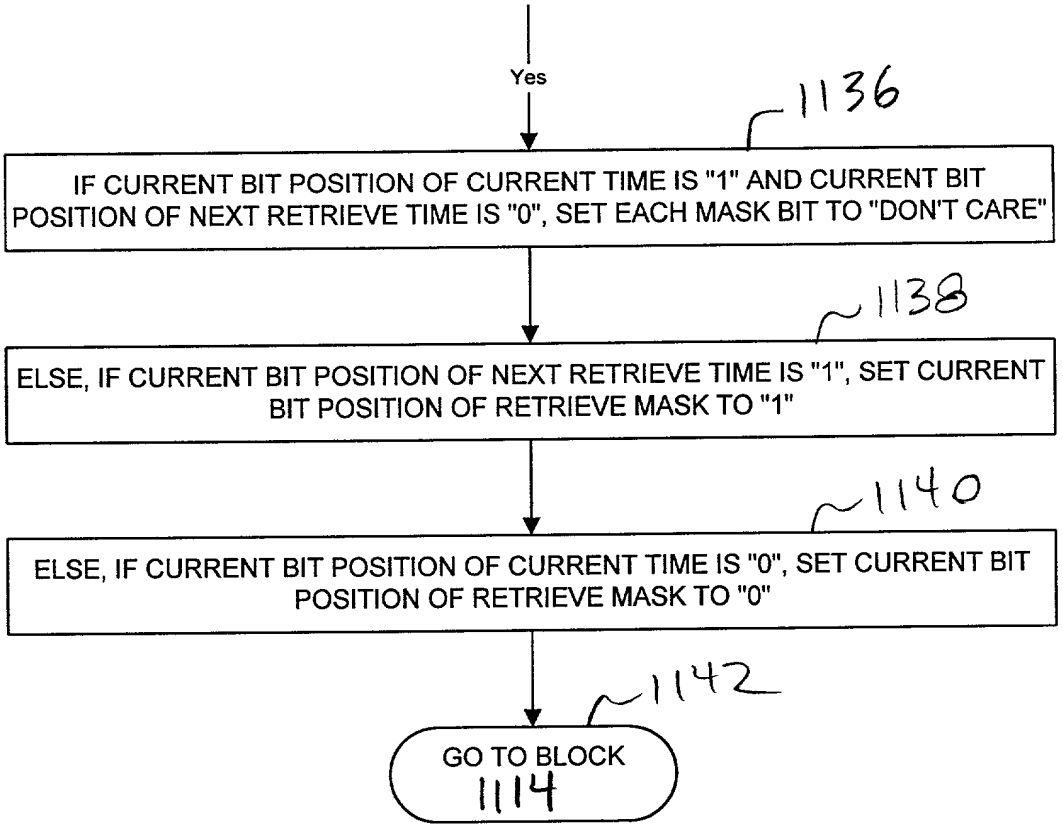
Yes
1136
IF CURRENT BIT POSITION OF CURRENT TIME IS "1" AND CURRENT BIT POSITION OF NEXT RETRIEVE TIME IS "0", SET EACH MASK BIT TO "DON'T CARE"
1138
ELSE, IF CURRENT BIT POSITION OF NEXT RETRIEVE TIME IS "1", SET CURRENT BIT POSITION OF RETRIEVE MASK TO "1"
1140
ELSE, IF CURRENT BIT POSITION OF CURRENT TIME IS "0", SET CURRENT BIT POSITION OF RETRIEVE MASK TO "0"
1142
GO TO BLOCK 1114

FIG. 11C